PA-1DC

QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	10/668,236	Prepared by	J. Escarcha	Tracking Number	05942756
Examiner-GAU	Tran - 2819	Date	5/19/04	Week Date	04/26/04
		No. of queries	1	HW T6	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE PTO 1449:

Please either initial or line through citation(s).

Thank you.

initials JLE

RESPONSE

initials

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 003921.00178	SERIAL NUMBER Div. of 09/404,920
	APPLICANT Frederic Reblewski et al.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE September 24, 2003	GROUP ART UNIT Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,642,487	02/1987	Carter			
	4,758,985	07/1988	Carter			
	5,036,473	07/1991	Butts			
	5,140,193	08/1992	Freeman, deceased et al.			
	5,701,441	12/1997	Trimberger, Stephen M.	326	39	
	5,943,490	08/1999	Sample			
	5,960,191	09/1999	Sample et al.	703	23	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Shibata, Y.; Miyazaki, H.; Xiao-Ping Ling; Amano, H., "Towards the realistic "virtual hardware," Innovative Architecture for Future Generation High-Performance Processors and Systems, 1997, 1998 pages: 50-55.
	Varghese, J.; Butts, M.; Batcheller, J., "An efficient logic emulation system," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 1 Issue: 2, June 1993 Pages: 171-174.
	Lo, W.Y.; Choy, C.S.; Chan, C.F., "Hardware emulation board based on FPGAs and Programmable Interconnections," Proceedings of the Fifth International Workshop on Rapid System Prototyping, 1994. Shortening the Path from Spec to Prototype. Pages 126-130.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.